We claim:

1. An apparatus comprising:

first and second execution cores to operate in an FRC mode;

an FRC check unit to compare results from the first and second execution cores and to store at least one result and a status to indicate if the results match;

an error check unit to assert a signal to the FRC checker if a recoverable error is detected in the first or second execution cores; and

a timer to trigger an FRC recovery routine if the status indicates the results do not match and the error check unit does not assert the signal within a specified interval.

2. The apparatus of claim 1, wherein the FRC checker stores a result from the master execution core and discards the result from the slave execution core.

3. The apparatus of claim 2, wherein the FRC checker stalls the slave execution core if the status indicates the results do not match and triggers a countdown to the specified interval.

4. The apparatus of claim 4, wherein the specified interval represents a time for a recoverable error to be signaled to the error detector.

5. The apparatus of claim 1, wherein the FRC check unit includes a multiple entry buffer to store results and status indicators for multiple.

6. The apparatus of claim 2, wherein a number of entries for the buffer is selected to determined by a largest number of clock cycle to propagate an error signal to the error detector.

7. The apparatus of claim 1, wherein the FRC check unit includes a buffer to store results from the first and second execution cores and their status.

8. The apparatus of claim 7, wherein the recovery routine reads an uncorrupted result from an appropriate entry of the buffer if the recoverable error is detected within the specified interval.

9. An system comprising:

first and second execution cores to operate in an FRC mode;

an FRC checker to compare results from the first and second execution cores and to trigger a countdown interval if the results do not match; and

an error detector to monitor error signals during the countdown interval and to disable the FRC checker if a recoverable error is detected before the countdown interval expires.

10. The system of claim 9, wherein the FRC checker includes a buffer to temporarily store results from at least one of the first and second execution cores.

11. The system of claim 9, wherein the FRC checker stalls one of the first and second execution cores if the results do not match.

12. The system of claim 9, further comprising a recovery unit to recover uncorrupted results from the first or second execution core, responsive to the error detector detecting a recoverable error.

13. The system of claim 12, further comprising a reset unit to reset the system, responsive to the FRC checker indicating an FRC error.

14. The system of claim 13, wherein the FRC checker indicates an FRC error if results from the first and second execution pipelines do not match and the FRC checker is not disabled before the countdown interval expires.

15. The system of claim 13, further comprising a memory device in which a recovery routine and a reset routine are stored.

16. The system of claim 15, wherein the recovery unit and the reset unit include pointers to the recovery routine and the reset routine, respectively.

17. A method comprising:

comparing results from a first and second execution core to detect an FRC error;

if the results do not match, setting a first flag and initiating a countdown interval;

monitoring an error signal for a recoverable error; and

initiating a recovery routine if the error signal is asserted before the countdown interval expires.

18. The method of claim 17, further comprising:

storing a result from at least one of the first and second execution cores; and

initiating a transaction to a shared resource if the first flag is not set.

19. The method of claim 18, further comprising initiating a reset routine if the error signal is not asserted before the countdown interval expires.

20. The method of claim 17, further comprising:

stalling one of the first and second execution cores if the first flag is set; and

continuing to monitor the error signal from the stalled execution core.